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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/699,528	10/31/2003	Ryo Nakagaki	16869N-099100US	4228
20350	7590	09/27/2005	EXAMINER	
TOWNSEND AND TOWNSEND AND CREW, LLP TWO EMBARCADERO CENTER EIGHTH FLOOR SAN FRANCISCO, CA 94111-3834			CHEN, KIN-CHAN	
		ART UNIT		PAPER NUMBER
		1765		

DATE MAILED: 09/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/699,528	NAKAGAKI ET AL.
Examiner	Art Unit	
Kin-Chan Chen	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 07 September 2005.

2a) This action is FINAL. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-15 is/are pending in the application.
4a) Of the above claim(s) 14,15 is/are withdrawn from consideration.
5) Claim(s) _____ is/are allowed.
6) Claim(s) 1-13 is/are rejected.
7) Claim(s) _____ is/are objected to.
8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) All b) Some * c) None of:
1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892)
2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 103103.
4) Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____.
5) Notice of Informal Patent Application (PTO-152)
6) Other: ____.

DETAILED ACTION

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Election/Restrictions

2. Applicant's election without traverse of claims 1-13 (September 7, 2005) is acknowledged.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

4. Claim 1 is rejected under 35 U.S.C. 102(a) as being anticipated by Muckenhirn (US 2003/0168594).

In a method and system for measuring microscopic surface features, Muckenhirm teaches that a test pattern and an actual circuit pattern on a semiconductor substrate may be formed by a predetermined semiconductor manufacturing process. A feature of the three-dimensional shape of said test pattern may be measured by use of an optical scatterometry apparatus. The semiconductor manufacturing process for the actual circuit pattern may be evaluated based on a result of the measurement. See [0002], [0003], Figs. 3 and 4; pages 5 and 8.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 2, 4-7, and 9-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Muckenhirm (US 2003/0168594) as evidenced by Bendik et al. (US 6,673,638), Singh et al. (US 6,778,268) and Yoshitake et al. (US 2003/0121022).

In a method and system for measuring microscopic surface features, Muckenhirm ([0002], [0003], [0065][0073], Figs. 3 and 4; pages 5 and 8) teaches that a test pattern and an actual circuit pattern on a semiconductor substrate may be formed by a predetermined semiconductor manufacturing process. A feature of the three-dimensional shape of said test pattern may be measured by use of an optical

scatterometry apparatus. The semiconductor manufacturing process for the actual circuit pattern may be evaluated based on a result of the measurement. Muckenhirk teaches monitoring the semiconductor manufacturing process. Muckenhirk teaches that the features are typically formed by photolithography process, making the process of exposure and development process (claims 2, 7) obvious, also see Bendik et al. (US 6,673,638; abstract, col. 2) as evidence. Muckenhirk teaches monitoring the semiconductor manufacturing process and a complete characterization of three-dimensional profile of the feature. Muckenhirk teaches measuring and generating library graphs, comparing with specification. Hence, it would have been obvious to one with ordinary skill in the art to perform calculation (such as manipulating data and performing calculation using various design rules, statistical methods e.g., regression, extrapolation, best-fit, fitting function) and prepare a correspondence relationship between test pattern and three-dimensional shape feature while varying the process parameter, and perform the evaluation. Muckenhirk also teaches AFM or SEM may be used for the measurement in combination with scatterometer. See also some calculations and data analysis examples in Singh et al. (US 6,778,268) and Yoshitake et al. (US 2003/0121022) as evidence.

7. Claims 3, 4-6, 8-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Muckenhirk (US 2003/0168594) as evidenced by Demmin (US 6,635,185), Singh et al. (US 6,778,268) and Yoshitake et al. (US 2003/0121022).

In a method and system for measuring microscopic surface features, Muckenhirn ([0002], [0003], [0065][0073], Figs. 3 and 4; pages 5 and 8) teaches that a test pattern and an actual circuit pattern on a semiconductor substrate may be formed by a predetermined semiconductor manufacturing process. A feature of the three-dimensional shape of said test pattern may be measured by use of an optical scatterometry apparatus. The semiconductor manufacturing process for the actual circuit pattern may be evaluated based on a result of the measurement. Muckenhirn teaches monitoring the semiconductor manufacturing process. Muckenhirn teaches monitoring the process parameters for forming holes contact holes, trench structures using etching process, making the changes of etching process parameters (e.g., claim 8) obvious, also see Demmin (US 6,635,185; col. 7, lines 5-25) as evidence. Muckenhirn teaches monitoring the semiconductor manufacturing process and a complete characterization of three-dimensional profile of the feature. Muckenhirn teaches measuring and generating library graphs, comparing with specification. Hence, it would have been obvious to one with ordinary skill in the art to perform calculation (such as manipulating data and performing calculation using various design rules, statistical methods e.g., regression, extrapolation, best-fit, fitting function) and prepare a correspondence relationship between test pattern and three-dimensional shape feature while varying the process parameter, and perform the evaluation. Muckenhirn also teaches AFM or SEM may be used for the measurement in combination with scatterometer. See also some calculations and data analysis examples in Singh et al. (US 6,778,268) and Yoshitake et al. (US 2003/0121022) as evidence.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Bendik et al. (US 6,673,638; abstract, col. 2) teach adjusting the exposure and development process in response to the measurements using SEM, AFM, and scatterometer. Singh et al. (US 6,778,268) and Yoshitake et al. (US 2003/0121022) perform calculation and data analysis using the measurements conducted by scatterometry. Demmin (US 6,635,185; col. 7, lines 5-25) discloses that one skilled in the art of plasma etching and cleaning may vary type of plasma etching (RIE, HDP, plasma etching..), composition, flow rate, temperature, pressure, power, time, bias, .. accordingly to etch a desired material satisfactorily.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kin-Chan Chen whose telephone number is (571) 272-1461. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on (571) 272-1465. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For

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more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

September 22, 2005



Kin-Chan Chen
Primary Examiner
Art Unit 1765